AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-10 (canceled)

Claim 11 (previously presented): The apparatus of claim 14, further comprising a frame buffer, wherein said processor stores image data in said frame buffer.

Claim 12 (previously presented): The apparatus of claim 14, wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data.

Claim 13 (previously presented): The apparatus of claim 14, wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer.

Claim 14 (currently amended): An apparatus for image processing, comprising:

a processor including a data decompression circuit;

a first storage device having texture data and electronically coupled to said processor; and

a texture buffer having decompressed texture data and electrically coupled to said processor; wherein

transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor; and

said first storage device is defined by a CPU work memory or an external memory device.

Claim ~~15~~ 5 (currently amended): An apparatus for image processing, comprising:

a processor including a data decompression circuit;

a first storage device having texture data and electronically coupled to said processor;

a texture buffer having decompressed texture data and electrically coupled to said processor; and

a first data bus and a second data bus, wherein said first data bus carries texture data between said texture buffer and said processor faster than said second data bus carries texture data from said storage device and said processor; and

said first storage device is defined by a CPU work memory or an external memory device.

Claim ~~16~~ 6 (previously presented): The apparatus of Claim ~~13~~ 4, wherein said processor including a FIFO storage device which temporarily stores said read compressed texture data.

Claim ~~17~~ 7 (previously presented): The apparatus of Claim ~~16~~ 6, wherein said data decompression circuit receives said read compressed texture data from said FIFO storage device.

Claim ~~18~~ 8 (previously presented): The apparatus of Claim ~~13~~ 4, wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decompressed texture data.

Claim ~~19~~ 9 (previously presented): The apparatus of Claim ~~13~~ 4, wherein said processor includes a mip map generation circuit, said mip map generation circuit

generating a mip map of said decompressed texture data.

Claim 20 (previously presented): The apparatus of claim 14, wherein said texture data in said first storage device is compressed.

Claim 21 (canceled)

Claim 22 (previously presented): The method of claim 23, further comprising the step of converting said decompressed texture data to image data, and storing said image data in a frame buffer.

Claim 23 (currently amended): An image processing method comprising the steps of:

providing compressed texture data in a storage device defined by a CPU work memory or an external memory device;

reading said compressed texture data from said storage device and decompressing said compressed texture data;

storing said decompressed texture data in a texture buffer; and

providing a processor, and transferring data between said texture buffer and said processor faster than transferring data between said storage device and said processor.

Claim 24 (previously presented): The method of claim 23, further comprising the step of performing palette conversion of said decompressed texture data prior to said step of storing said texture data.

Claim 25 (previously presented): The method of Claim 23, further comprising the step of generating a mip map of said compressed texture data prior to said step of storing said decompressed texture data.

Claim 26 (previously presented): The method of claim 23, wherein said step of storing said decompressed texture data includes the step of updating said decompressed texture data in said texture buffer with new decompressed texture data.

Claim 27 (previously presented): The apparatus of claim 15, further comprising a frame buffer, wherein said processor stores image data in said frame buffer.

Claim 28 (previously presented): The apparatus of claim 15, wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data.

Claim 29 (previously presented): The apparatus of claim 15, wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer.

Claim 30 (previously presented): The apparatus of claim 29, wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data.

Claim 31 (previously presented): The apparatus of claim 30, wherein said data decompression circuit receives said read compressed texture data from said FIFO storage device.

Claim 32 (previously presented): The apparatus of claim 29, wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decompressed texture data.

Claim 33 (previously presented): The apparatus of claim 29, wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed texture data.

Claim 34 (previously presented): The apparatus of claim 15, wherein said texture data in said first storage device is compressed.